Understanding MAX 9000 Timing

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Introduction

Altera® devices provide predictable device performance that is consistent from simulation to application. Before placing a device in a circuit, you can determine the worst-case timing delays for any design. You can calculate propagation delays either with the MAX+PLUS® II Timing Analyzer or with the timing models given in this application note and the timing parameters listed in the *MAX 9000 Programmable Logic Device Family Data Sheet* in this data book.

For the most precise timing results, you should use the MAX+PLUS II Timing Analyzer, which accounts for the effects of secondary factors such as placement and fan-out.

This application note defines MAX® 9000 device internal and external timing parameters, and illustrates the timing model for the MAX 9000 device family. The timing information in this document also applies to MAX 9000A devices.

Familiarity with MAX 9000 architecture and characteristics is assumed. Refer to the *MAX 9000 Programmable Logic Device Family Data Sheet* for a complete description of the MAX 9000 architecture, and for the specific values of the timing parameters listed in this application note.

Internal Timing Parameters

The timing delays contributed by individual MAX 9000 architectural elements are called internal timing parameters, which cannot be measured explicitly. All internal timing parameters are shown in italic type. The following list defines the internal timing parameters for the MAX 9000 device family.

t_{INCOMB} I/O input pad and buffer delay. This delay applies to I/O pins used as inputs, and represents the time required for a signal on an I/O pin to reach a row or column interconnect on the FastTrack™ Interconnect.

t_{INREG} I/O input pad to I/O register delay. This delay applies to I/O pins used as inputs, and represents the time required for a signal on an I/O pin to reach the data input of an I/O register.

t_{DIN_D}	Dedicated input data delay. This delay represents the time required for a signal originating from a dedicated input pin and used as a data input to a macrocell to reach a row interconnect on the FastTrack Interconnect.
t_{DIN_CLK}	Dedicated input clock delay. The delay for a signal that originates from a dedicated input pin and is used as a macrocell register clock.
t_{DIN_CLR}	Dedicated input clear delay. The delay for a signal that originates from a dedicated input pin and is used as a macrocell register clear.
t_{DIN_IO}	Dedicated input I/O control delay. The delay for a signal that originates from a dedicated input pin (including the enable and clear inputs to the I/O register, and the output enable control of the I/O cell's tri-state buffer) and is used as an I/O register control.
t_{DIN_IOC}	Dedicated input I/O clock delay. The delay for a signal that originates from a dedicated input pin and is used as an I/O register clock.
t_{COL}	FastTrack Interconnect column delay. The delay incurred by a signal that requires routing through a column interconnect. The t_{COL} delay is a function of fan-out and of the distance between the source and destination macrocells. t_{COL} is a worst-case value for most column signals.
t_{ROW}	FastTrack Interconnect row delay. The delay incurred by a signal that requires routing through a row interconnect. The t_{ROW} delay is a function of fan-out and of the distance between the source and destination macrocells. t_{ROW} is a worst-case value for most row signals.
t_{LOCAL}	Logic array block (LAB) local array delay. The delay incurred by a signal that is routed from one macrocell to another macrocell in the same LAB.
t_{LAD}	Logic array delay. The time required for a logic signal to propagate through a macrocell's AND-OR-XOR structure.
t_{LAC}	Logic array control delay. The AND array delay for register control functions, including the clear and preset inputs to the macrocell register.

t_{IC}	Array clock delay. The delay through a macrocell's clock product term to the register's clock input.
t_{EN}	Register enable delay. The AND array delay for the macrocell register enable.
t_{SEXP}	Shared expander delay. The delay of a signal through the AND-NOT structure of the shared expander product-term array that is fed back into the local array.
t_{PEXP}	Parallel expander delay. The additional delay incurred by adding parallel expander product terms to the macrocell product terms. An additional t_{PEXP} delay is added to the timing path for each group of up to five parallel expanders added to a macrocell.
t_{RD}	Macrocell clock-to-output delay. The delay from the rising edge of the macrocell register's clock to the time the data appears at the register output.
t_{COMB}	Macrocell combinatorial output delay. The delay required for a signal to bypass the macrocell register and become the macrocell output.
t_{SU}	Macrocell register setup time. The time required for a signal to be stable at the macrocell register input before the register clock's rising edge to ensure that the register correctly stores the input data.
t_{H}	Macrocell register hold time. The time required for a signal to be stable at the macrocell register input after the register clock's rising edge to ensure that the register correctly stores the input data.
t_{PRE}	Macrocell register preset delay. The delay from the assertion of the macrocell register's asynchronous preset input to the stabilization of the register output at logical high.
t_{CLR}	Macrocell register clear delay. The delay from the assertion of the macrocell register's clear input to the stabilization of the register output at logical low.
t_{FTD}	FastTrack Interconnect drive delay. The delay from the time when a signal is available on the macrocell output to the time that signal is driven onto the row or column interconnect.

t_{IODR}	Output data delay for the row. The delay incurred by signals routed from a row to an I/O cell.
t_{IODC}	Output data delay for the column. The delay incurred by signals routed from a column to an I/O cell.
t_{IOC}	I/O cell control delay. The delay incurred by a signal that requires routing on the peripheral bus and controls the I/O register's enable or clear input or controls the output enable of the I/O cell's tri-state buffer. The t_{IOC} delay is a function of fan-out and the distance between the source row and the destination I/O cells (IOCs). The t_{IOC} delay is a worst-case value for a fan-out of 8.
t_{IORD}	I/O register clock-to-output delay. The delay from the rising edge of the I/O register's clock to the time the data appears at the register output.
t_{IOCOMB}	I/O register bypass delay. The delay for a signal to bypass the I/O register.
t_{IOSU}	I/O register setup time. The time required for a signal to be stable at the I/O register input before the register clock's rising edge to ensure that the register correctly stores the input data.
t_{IOH}	I/O register hold time. The time required for a signal to be stable at the I/O register input after the register clock's rising edge to ensure that the register correctly stores the input data.
t_{IOCLR}	I/O register clear delay. The delay from the time when the I/O register's asynchronous clear input is asserted to the time the register output stabilizes at logical low.
t_{IOFD}	I/O register feedback delay. The delay from the output of the I/O register to the row or column interconnect.
t_{OD1}	Output buffer and pad delay with the slow slew rate logic option turned off and V_{CCIO} = 5.0 V.
t_{OD2}	Output buffer and pad delay with the slow slew rate logic option turned off and V_{CCIO} = 3.3 V.
t_{OD3}	Output buffer and pad delay with the slow slew rate logic option turned on and V_{CCIO} = 3.3 V or 5.0 V.

t_{XZ} Output buffer disable delay. The delay required for high impedance to appear at the output pin after the tri-state buffer's enable control is disabled.

t_{ZX1} Output buffer enable delay with the slow slew rate logic option turned off and V_{CCIO} = 5.0 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled.

t_{ZX2} Output buffer enable delay with the slow slew rate logic option turned off and V_{CCIO} = 3.3 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled.

t_{ZX3} Output buffer enable delay with the slow slew rate logic option turned on and V_{CCIO} = 5.0 V or 3.3 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled.

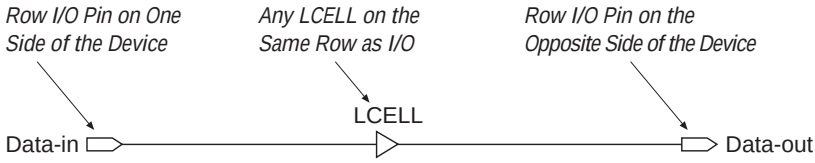
t_{LPA} Low-power adder. The delay associated with macrocells in low-power operation. In low-power mode, t_{LPA} must be added to the LAB local array delay (t_{LOCAL}).

External Timing Parameters

External timing parameters represent actual pin-to-pin timing characteristics. Each external timing parameter consists of a combination of internal timing parameters. The *MAX 9000 Programmable Logic Device Family Data Sheet* gives the values of the external timing parameters. These external timing parameters are worst-case values, derived from extensive performance measurements and ensured by device testing. All external timing parameters are shown in bold type. The following list defines external timing parameters for the MAX 9000 family.

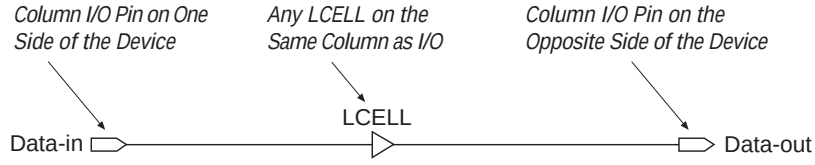
t_{PD1} Row I/O pin to non-registered row pin delay. The time required for a signal on any row input to propagate through the combinatorial logic in a macrocell and appear at a row output pin. The test circuit for this parameter is a row input pin on one side of the device that feeds a row output on the opposite side of the device through an LCELL in that row. See Figure 1.

Figure 1. Test Circuit for t_{PD1}



t_{PD2} Column I/O pin to non-registered column pin delay. The time required for a signal on any column input to propagate through the combinatorial logic in a macrocell and appear at a column output pin. The test circuit for this parameter is a column input pin on one side of the device that feeds a column output on the opposite side of the device through an LCELL in that column. See Figure 2.

Figure 2. Test Circuit for t_{PD2}



t_{FSU} Global clock setup time for I/O cell register. The time the input data must be present at the I/O pin before the global (synchronous) clock signal is asserted at the clock pin.

t_{FH} Global clock hold time for I/O cell register. The time the input data must be present at the I/O pin after the global clock signal is asserted at the clock pin.

t_{CO} Global clock to output delay for macrocell registers. The time required to obtain a valid row output after the global clock is asserted at the clock pin.

t_{FCO} Global clock to output delay for I/O cell register. The time required to obtain a valid output after the global clock is asserted at the clock pin.

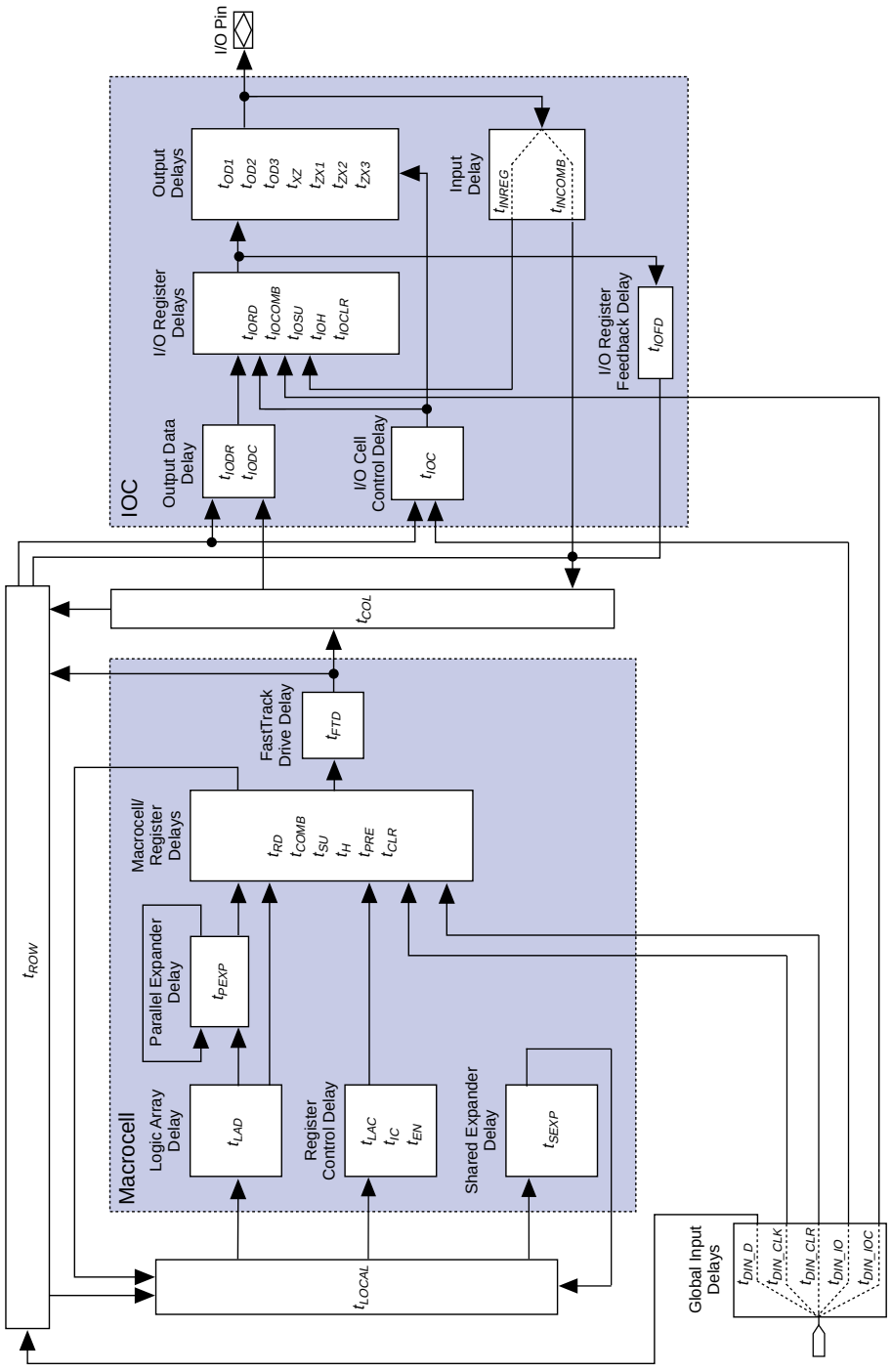
t_{CNT} Minimum global clock period. The minimum period maintained by a globally clocked, 16-bit loadable, enabled, up/down counter.

t_{ACNT}	Minimum array clock period. The minimum period maintained by a 16-bit loadable, enabled, up / down counter when it is clocked by a signal from the array.

MAX 9000 Timing Model

Timing models are simplified block diagrams that illustrate the propagation delays through Altera devices. Logic can be implemented on different paths. You can trace the actual paths used in your MAX 9000 device by examining the equations listed in the MAX+PLUS II Report File (**.rpt**) for the project. You can then add up the appropriate internal timing parameters to calculate the approximate propagation delays through the MAX 9000 device. However, the MAX+PLUS II Timing Analyzer provides the most accurate timing information. Figure 3 shows the timing model for MAX 9000 devices.

Figure 3. MAX 9000 Timing Model



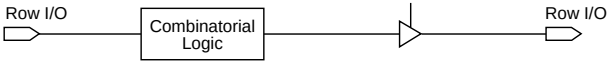
Calculating Timing Delays

You can calculate approximate pin-to-pin timing delays for MAX 9000 devices with the timing model shown in Figure 3 and the internal timing parameters in the *MAX 9000 Programmable Logic Device Family Data Sheet* in this data book. Each external timing parameter is calculated from a combination of internal timing parameters. Figure 4 shows the MAX 9000 device family macrocell external timing parameters. To calculate the delay for a signal that follows a different path through the MAX 9000 device, refer to the timing model to determine which internal timing parameters to add together.

Figure 4. Macrocell External Timing Parameters (Part 1 of 3)

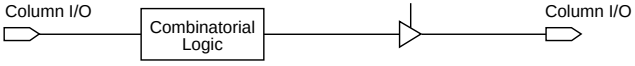
Combinatorial Delay

From Row I/O Inputs to Row I/O Outputs:



$$t_{PD1} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$$

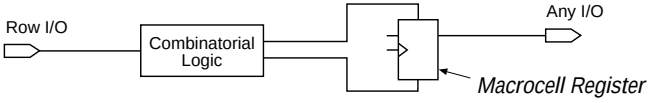
From Column I/O Inputs to Column I/O Outputs:



$$t_{PD2} = t_{INCOMB} + t_{COL} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{COL} + t_{IODC} + t_{IOCOMB} + t_{OD1}$$

Macrocell Register Clear & Preset Time

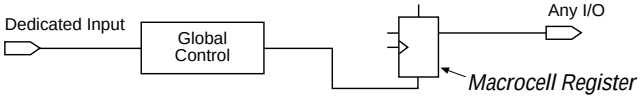
From Row I/O Inputs to Row or Column Outputs:



$$t_{CLR} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAC} + t_{CLR} + t_{FTD} + (t_{ROW} \text{ or } t_{COL}) + (t_{IODR} \text{ or } t_{IODC}) + t_{IOCOMB} + t_{OD1}$$

$$t_{PRE} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAC} + t_{PRE} + t_{FTD} + (t_{ROW} \text{ or } t_{COL}) + (t_{IODR} \text{ or } t_{IODC}) + t_{IOCOMB} + t_{OD1}$$

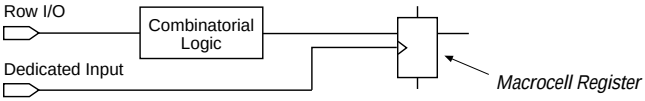
From Dedicated Inputs to Row or Column Outputs:



$$t_{CLR} = t_{DIN\_CLR} + t_{CLR} + t_{FTD} + (t_{ROW} \text{ or } t_{COL}) + (t_{IODR} \text{ or } t_{IODC}) + t_{IOCOMB} + t_{OD1}$$

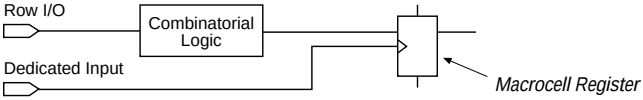
Figure 4. Macrocell External Timing Parameters (Part 2 of 3)

Register Setup Time from a Global Clock & Row I/O Data Input



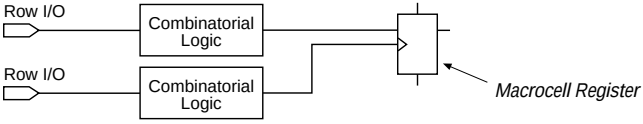
$$t_{SU} = (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD}) - t_{DIN\_CLK} + t_{SU}$$

Register Hold Time from a Global Clock & Row I/O Data Input



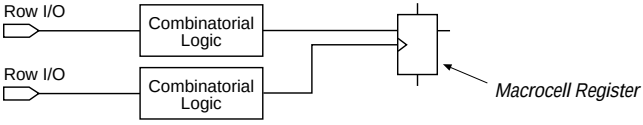
$$t_{H} = t_{DIN\_CLK} - (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD}) + t_{H}$$

Asynchronous Setup Time from a Row I/O Clock & Row I/O Data Input



$$t_{ASU} = (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD}) - (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{IC}) + t_{SU}$$

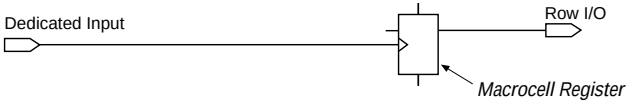
Asynchronous Hold Time from a Row I/O Clock & Row I/O Data Input



$$t_{AH} = (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{IC}) - (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD}) + t_{H}$$

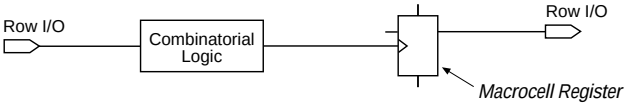
Figure 4. Macrocell External Timing Parameters (Part 3 of 3)

Clock-to-Output Delay from a Global Clock & Row Output



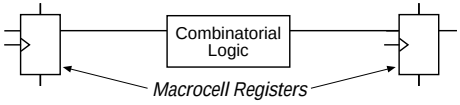
$$t_{CO} = t_{DIN\_CLK} + t_{RD} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$$

Asynchronous Clock-to-Output Delay from a Row I/O Clock & Row Output



$$t_{ACO} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{IC} + t_{RD} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$$

Counter Frequency



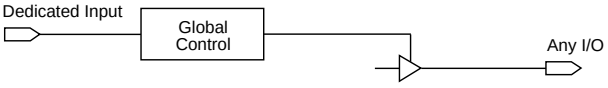
$$t_{CNT} = t_{RD} + t_{LOCAL} + t_{LAD} + t_{SU}$$

Figure 5 shows the MAX 9000 device family I/O cell (IOC) external timing parameters. To calculate the delay for a signal that follows a different path through the device, refer to the MAX 9000 timing model shown in Figure 3 on page 612 to determine which internal timing parameters to add together.

Figure 5. I/O Cell External Timing Parameters (Part 1 of 2)

Tri-State Enable & Disable Delay

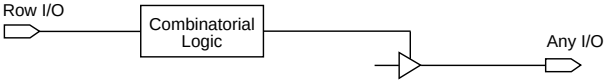
For Global Output Enable:



$t_{ZX} = t_{DIN\_IO} + t_{IOC} + t_{ZX1}$

$t_{XZ} = t_{DIN\_IO} + t_{IOC} + t_{XZ}$

For Row Output Enable:

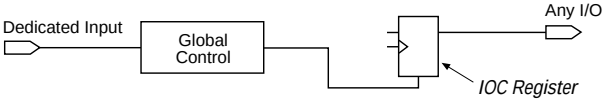


$t_{PZX} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC} + t_{ZX1}$

$t_{PXZ} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC} + t_{XZ}$

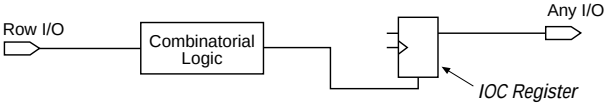
I/O Register Clear Time

From Dedicated Inputs:



$t_{CLR} = t_{DIN\_IO} + t_{IOC} + t_{IOCLR} + t_{OD1}$

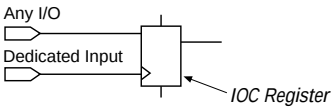
From Row I/O Inputs:



$t_{CLR} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC} + t_{IOCLR} + t_{OD1}$

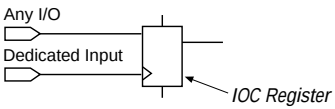
Figure 5. I/O Cell External Timing Parameters (Part 2 of 2)

Register Setup Time from a Global Clock



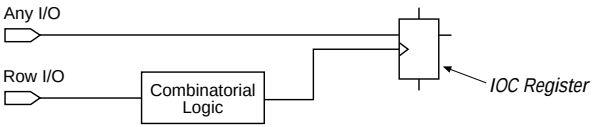
$t_{FSU} = t_{INREG} - t_{DIN\_IOC} + t_{IOSU}$

Register Hold Time from a Global Clock



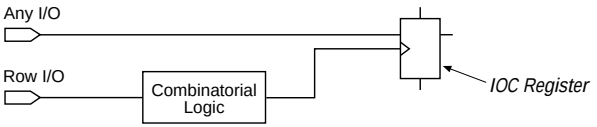
$t_{FH} = t_{DIN\_IOC} - t_{INREG} + t_{IOH}$

Asynchronous Setup Time from a Row I/O Clock



$t_{FASU} = t_{INREG} - (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC}) + t_{IOSU}$

Asynchronous Hold Time from a Row I/O Clock



$t_{FAH} = (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC}) - t_{INREG} + t_{IOH}$

Timing Model vs. MAX+PLUS II Timing Analyzer

The MAX+PLUS II Timing Analyzer always provides the most accurate information on the performance of a design. However, hand calculations based on the timing model also provide a good estimate of the design performance. The MAX+PLUS II Timing Analyzer is more accurate because it takes into account two factors that affect the t_{ROW}, t_{COL}, and t_{IOC} internal timing parameters:

- Fan-out for each signal in the delay path
- Distance between signal source and destination

Fan-Out

The more loads a signal has to drive, the longer the delay across t_{ROW}, t_{COL}, and t_{IOC}. For t_{ROW}, this loading is a function of the number of LABs that a signal source has to drive. For t_{COL}, this loading is a function of the number of rows that a signal source has to reach. For t_{IOC}, this loading is a function of the number of IOCs that a signal source controls. For example, consider a signal `s1` going to destination `d1` that also goes to macrocells `y[4..1]`. If `y[4..1]` are in different LABs, then `s1` has four loads. If, however, they are all in the same LAB,`s1` has only one load. Therefore, the row interconnect delay from `s1` to `d1` is greater when each macrocell `y[4..1]` is in a different LAB. The same is true for a column delay. If `y[4..1]` are in different rows, the delay will be longer than if they are in the same row.

Distance

The distance between the source and destination also affects the t_{ROW}, t_{COL}, and t_{IOC} parameters. For example, if `s1` and `d1` are pins on the left and right sides of a device, respectively, the delay from `s1` through one `LCELL` on the same row to `d1` (i.e., the time required to traverse the length of the device) is the same no matter where the `LCELL` is placed. On the other hand, if `s1` and `d1` are both on the same side, the delay from `s1` to `d1` depends on where the `LCELL` is placed. If the `LCELL` is on the opposite side from `s1` and `d1`, the delay is longer than if the `LCELL` is on the same side as `s1` and `d1`. The same is true for the delay incurred by traversing a column. For t_{IOC}, as the IOC becomes farther away from the source row, the delay incurred by traversing the peripheral bus increases.

Examples

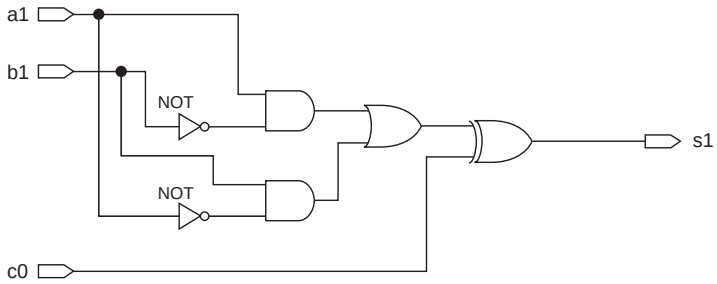
The following examples show how to use internal timing parameters to estimate the delays for real applications.

Example 1: First Bit of a 7483 TTL Macrofunction

You can analyze the timing delays for circuits that have been subjected to minimization and logic synthesis. A MAX+PLUS II Report File (**.rpt**) lists the synthesized equations for the project. These equations are structured so that you can quickly determine the logic implementation of any signal. Figure 6 shows part of a 7483 TTL macrofunction (a 4-bit full adder). The Report File for this TTL macrofunction circuit gives the following equations for `s1`, the least significant bit (LSB) of the adder:

```
% s1       = _LC9_B1 %
s1         = LCELL(_EQ002 $ c0);
_EQ002     = !a1 &  b1
           #  a1 & !b1;
```

Figure 6. Adder Logic Timing for MAX 9000 Architecture



The s1 output is the output of macrocell 9 in LAB b1 (_LC9_B1), which contains combinatorial logic. The combinatorial logic LCELL (_EQ002 $ c0) represents the XOR of the intermediate equation _EQ002 and the carry-in c0. In turn, _EQ002 is logically equivalent to the XOR of inputs b1 and a1. Therefore, the timing delay for s1 can be estimated by adding the following parameters:

$t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$

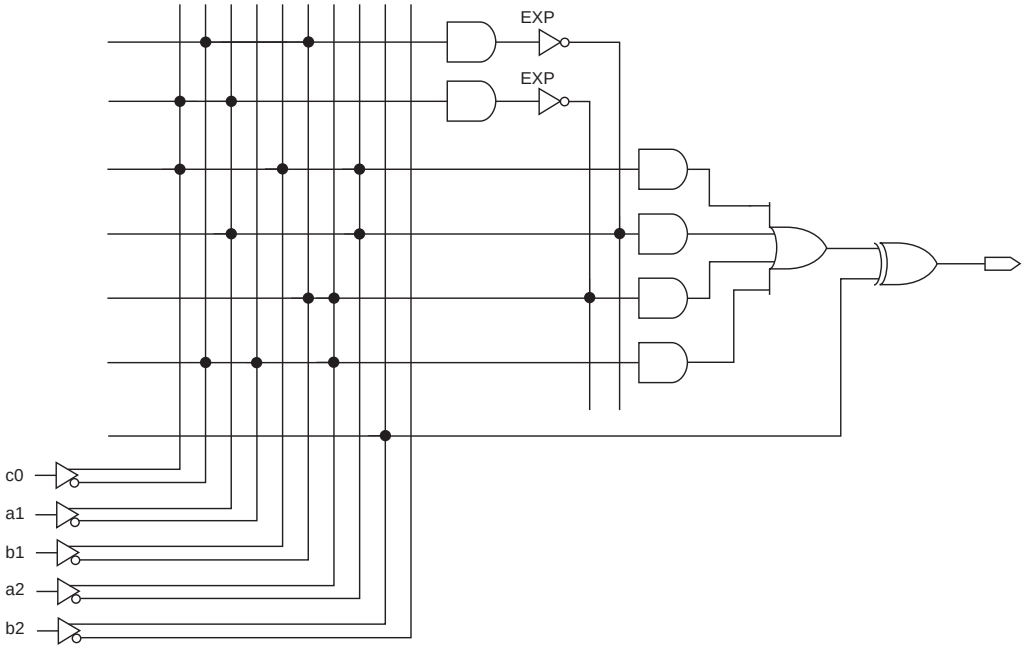
Example 2: Second Bit of a 7483 TTL Macrofunction

The expander array delay, t_{SEXP}, is added to the delay element for complex logic that requires expanders (represented as _X<*number*> in Report Files). The second bit of the 7483 adder macrofunction, s2, requires shared expanders. The equations are as follows:

```
% s2       = _LC8_B1 %
s2         = LCELL(_EQ003 $ b2);
_EQ003     = !a2 &  b1 &  c0
           #  a1 & !a2 &  _X005
           #  a2 & !b1 &  _X006
           # !a1 & a2 & !c0;
_X005      = EXP(!b1 & !c0);
_X006      = EXP( a1 &  c0);
```

Figure 7 shows how to map the logic structure onto the MAX 9000 architecture with this equation.

Figure 7. Adder Equations Mapped to MAX 9000 Architecture



Therefore, the timing delay for s2 can be estimated by adding the following parameters:

$t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{SEXP} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$

Example 3: Second Bit of a 7483 TTL Macrofunction with Parallel Expanders

The MAX+PLUS II Compiler uses parallel expanders if the Parallel Expanders logic option is turned on when a project is compiled for MAX 9000 devices. When parallel expanders are used and no sharable expanders are used, the equation for s2 is as follows:

```
% _LC10_B1 borrows parallel expanders from _LC9_B1 %
% s2      = _LC10_B1 %
s2        = LCELL(_EQ003 $ b2);
_EQ003    =  a1 & !a2 &  c0
          #  a1 & !a2 &  b1
          # !a2 &  b1 &  c0
          # !a1 &  a2 & !b1
          #  a2 & !b1 & !c0
          # !a1 &  a2 & !c0;
```

Therefore, the timing delay for the s2 bit of the 7483 adder macrofunction can be estimated by adding the following parameters:

$$t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{PEXP} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$$

Example 4: First Bit of 7483 TTL Macrofunction in Low-Power Mode

If a macrocell in a MAX 9000 device is set for low-power mode, you must add the low-power adder delay to the total delay through that macrocell. The estimated s1 delay becomes:

$$t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LPA} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$$

Conclusion

The MAX 9000 device architecture has predictable internal timing delays that can be estimated based on signal synthesis and placement. Using the MAX 9000 timing model shown in Figure 3 on page 612 and the timing parameters in the *MAX 9000 Programmable Logic Device Family Data Sheet* in this data book, you can estimate the performance of a design before compilation. However, the MAX+PLUS II Timing Analyzer provides the most accurate timing information. These two methods enable you to accurately predict your design's in-system timing performance.

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